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ART UNIT	PAPER NUMBER
2111	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/583,397	XIONG, XIAOKUN	
	Examiner	Art Unit	
	BRIAN T. MISIURA	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☒ Claim(s) *6,8,9 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 December 2010* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

Response to Arguments

1. Applicant's amendments to the Drawings and Specification have successfully overcome their previous objections.

2. Claims 1, 6, 8, 9, 10, 11, and 13 have been amended to overcome 35 USC § second paragraph antecedent basis issues and therefore said rejections have been withdrawn.

3. Page 8 of the Remarks comprises the Applicants argument regarding the indefiniteness of the limitation "i960-like". The Applicant points to page 1 lines 22-24 of the specification that states

> i960 is a series of microprocessors provided by Intel company for the embedded applications, and there are a lot of interface devices right now based upon i960 or i960-like bus interface protocol. One skilled in the art would understand that an "i960-like" interface means an interface based on the i960 or i960-like bus interface protocol.

4. The Examiner respectfully disagrees that the cited specification section successfully defines the term "i960-like". The term "i960-like" is not commonly known in the art like the term i960 is. The above citation attempts to define "i960-like" as an interface based on the i960 or i960-like bus interface protocol. However, the term i960-like is not properly defined and therefore an i960-like interface can not be defined as an interface based on the i960-like bus interface protocol.

5. Further clarification is still required in defining the term "i960-like". For example, as broadly presented, an i960-like bus protocol can be considered any protocol that shares a common feature as the i960 bus protocol. For example, an i960 bus is well known to be an embedded processor bus (based on the i960 series of microprocessors

provided by Intel for embedded applications, see applicants specification "background"), and therefore, the embedded processor busses of Lupien (column 2 lines 22-30) are considered "i960-like".

6. Applicant's arguments filed 12/8/2010 regarding the 35 USC § 103(a) rejections have been fully considered but they are not persuasive.

7. Pages 9 and 10 of the Remarks comprise the arguments regarding the rejection of claim 1 (see Remarks for full citation).

8. The Examiner respectfully disagrees with the arguments. Lupien Jr. does in fact teach/suggest a main controller (**bridge 100**) for accomplishing bus protocol conversion between an AHB interface and an i960-like interface (**Column 2 states the busses may be embedded processor busses. Column 14 states one of the busses may be an AHB bus. As explained above, an embedded processor bus can be considered an i960-like bus. The bridge performs bus conversion as disclosed @ column 3 lines 50-59 and column 12 last paragraph**).

9. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "specific logical circuit structures") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

10. It is unclear if the Applicant is referring to the AHB and i960-like interfaces in the argument "Lupien Jr. fails to teach or suggest logical circuit structures for connecting the busses". However, the claims do not claim any "logical circuit structures" outside of the AHB and i960-like interfaces that have been taught by Lupien Jr. as mapped below.

11. Further, the Applicant argues, "In fact, the bridge 100 in Lupien et al. is merely a general bridge and does not suggest the structure of a main controller as required by claim 1." The Examiner notes that the claim only comprises the following limitations regarding the main controller: "a main controller for accomplishing bus protocol conversion between the AHB interface and the i960-like interface." Therefore, the only requirement of the main controller limitation is a "structure" that accomplishes the claimed bus protocol conversion.

12. The further Applicant arguments regarding Lupien Jr. not disclosing an i960-like bus have been addressed above regarding the indefiniteness of the term i960-like.

13. Regarding the arguments on pages 10 and 11 regarding claim 4, the Examiner highlights the write buffer enable (WBE) bits of Table 1.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

14. Claims 1-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

15. The term "i960-like" is a relative term which renders the claim indefinite. The term "i960-like" is not definite by the claim, the specification does not provide a standard for ascertaining the requisite degree to which a bus protocol qualifies as "i960-like", and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

16. Claims 1 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lupien Jr. et al. U.S. Patent No. 6,996,659 in view of Ezzet, U.S. Patent No. 5,603,051.

17. Per claim 1, Lupien Jr. discloses: a bus interface converter capable of converting AMBA AHB bus protocol into i960-like bus protocol (**Column 2 lines 22-39 and Figure 1 discloses that the busses may comprise embedded processor busses. An embedded processor bus is considered one of the broadly claimed "i960-like" bus protocols. Column 14 last paragraph and Figure 10 disclose an AHB bus. For the remainder of the reference citations, Bus 1 of Lupien will refer to the AHB bus and Bus 2 of Lupien will refer to an "i960-like" bus.**), wherein the converter comprising: an AHB interface for accomplishing interface processing for AMBA AHB bus protocol (**Figure 1; Bus 1 specific logic 106**); an i960-like interface for accomplishing interface processing for i960-like bus protocol (**Figure 1; Bus 2 specific logic 108**); and a main controller for accomplishing bus protocol conversion between the AHB interface and the i960-like interface (**Figure 1, Bridge 100 comprises routing manager 162. Column 12 last paragraph, Figure 9.**); wherein, the AHB interface

comprising: an AHB bus signal register module for accomplishing judgment and register for control signal from an AMBA AHB bus (**Column 3 lines 15-33, Figure 2; Bus 1 master sequencer 116a**); and an AHB bus signal response module for generating corresponding response indicating signal of AMBA AHB bus protocol (**Column 4 lines 25-37, Figure 2; Bus slave sequencer 116b**); the i960-like interface comprising: a bus interface multiplexing request module for generating bus interface multiplexing request signal (**Column 4 lines 6-24 and last paragraph, Figure 2; Bus 2 master sequencer 126a**); and a bus multiplexing module for accomplishing the multiplexing between the address bus for outputting from AHB to i960-like and the data bus for outputting from AHB to i960-like (**Column 9 line 59 – Column 10 line 6; Figure 4 numeral 170b**).

Lupien Jr. discloses a generic bridge for coupling two or more busses; and wherein the busses may comprise embedded processor busses. The disclosure of Lupien Jr. is presented with the first bus being an AHB bus and the second bus being a PCI-X bus (Figure 10). Lupien Jr. does not specifically mention "i960" in the disclosure but it is well known in the art that i960 refers to a RISC-based processor from Intel and thus an embedded processor bus is considered an i960-like bus.

However, for full disclosure, Ezzet is provided to teach that it is well known in the art for an i960 bus protocol to be coupled to a second bus protocol via a bridging circuit (**Column 6 last paragraph, Figure 5**).

- It would have been obvious to one having ordinary skill in the art at the time the invention was made to use an i960 protocol bus as taught by Ezzet as the second bus of Lupien Jr. because it qualifies as an embedded processor bus. Additionally, both Lupien Jr. and Ezzet are from the same field of endeavor (different protocol bus bridging).

18. Per claim 7, Lupien Jr. discloses the converter according to claim 1, wherein the i960-like interface can be directly connected to i960-like bus (**Figure 1 numerals 108 and 104**).

19. Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lupien Jr. et al. U.S. Patent No. 6,996,659 in view of Ezzet, U.S. Patent No. 5,603,051 in further view of Jahnke et al. U.S. Patent No. 6,829,669.

20. Per claim 2, Lupien Jr. discloses data buffers 166, but does not specifically disclose the limitations of claim 2.

However, Jahnke discloses an AHB to HTB (high performance data transfer bus) bus bridge 315 that includes a write buffer (**FIFO's 510 and 520**) for latching the full address and data from the AHB bus 300 (**Column 4 last paragraph, Figures 3 and 5**).

- It would have been obvious to one having ordinary skill in the art at the time of the applicants claimed invention to implement the data/address write buffers of Jahnke within the buffering scheme of Lupien Jr. because the AHB bus comprises both address and data busses and both the address and data information are necessary for completing the transaction.

21. Per claim 3, Jahnke further discloses wherein the AHB bus write buffer module comprises two buffering fields: address field and data field (**Column 4 last paragraph; Address FIFO 510 and Data FIFO 520**). Please refer to claim 2 for motivation to combine the references.

22. Per claim 4, Jahnke further discloses wherein the AHB bus write buffer module has an enabling port, and can set the size of buffering fields for the address field and data field of the AHB bus write buffer module via AHB bus (**Column 6 table 1**). Please

refer to claim 2 for motivation to combine the references.

23. Claims 5 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lupien Jr. et al. U.S. Patent No. 6,996,659 in view of Ezzet, U.S. Patent No. 5,603,051 in further view of Stewart, U.S. Patent No. 6,789,153.

24. Per claim 5, Lupien Jr. does not specifically disclose the HREADYout and HRESP signals.

However, Stewart discloses a plurality of signals that pass through AHB bus bridge 20, including HREADYout and HRESP signals (**Table 1**).

- It would have been obvious to one having ordinary skill in the art at the time of the applicants claimed invention for the AHB specification signals as disclosed by Stewart to be utilized within the AHB system of Lupien Jr. since the signals are inherent to the protocols specification.

25. Per claim 12, Lupien Jr. does not specifically disclose a state machine.

However, Stewart discloses AHB bus bridge 20 comprising a state machine 51 where the state machine controls the overall function of the bridge (**Column 5 lines 10-16**). Stewart further discloses that the state machine includes the three states of idle, read, and write (**Figure 7**).

- It would have been obvious to one having ordinary skill in the art at the time of the applicants claimed invention for the bridging circuitry of Lupien Jr. to include a state machine like that of Stewart because it controls the overall function of a bridging circuit by performing functions as they were designed in an attempt to avoid error conditions.

26. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lupien Jr. et al. U.S. Patent No. 6,996,659 in view of Ezzet, U.S. Patent No. 5,603,051 in further view of Fuks U.S. Patent No. 7,165,184.

27. Per Claim 10, Lupien Jr. does not specifically disclose wherein the main controller has two clocks being synchronous with AHB bus clock and i960-like bus clock respectively.

However, Fuks discloses bridging two different bus protocols via a bridge 30, where the each of the busses clock domains are utilized in latching data from the respective buses (**Column 2 lines 6-23**).

- It would have been obvious to one having ordinary skill in the art at the time of the applicants claimed invention to implement the bus clock domain functionality of the bridge of Fuks within the bridging circuit of Lupien Jr. because it is less expensive to implement than independent clock schemes which require additional remapping circuitry.

28. Per Claim 11, Lupien Jr. does not specifically disclose the relationship of the clock frequencies of the two busses being bridged.

However, Fuks discloses wherein the clock frequency of a first bus may be N times of that of the a second bus, where N is a natural number no less than 1 (**Column 3 lines 32-54; AHB bus 20 may be 78 MHz which is 6 times greater than the LPFAB bus 28 at 13 MHz**).

- It would have been obvious to one having ordinary skill in the art at the time of the applicants claimed invention for a first bus to have a frequency N times greater than

a second bus it is being bridged to because systems comprises a plurality of busses of varying frequencies based upon what their intended functioning is.

Allowable Subject Matter

29. Claim 13 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action. Reasons for allowance were previously presented in the Non-Final Rejection (12/8/2010) at numerals 34-37.

30. Claims 6, 8, and 9 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

31. Claims 6, 8, and 9 are considered to be containing allowable subject matter in light of their new interpretation based on the claim amendments presented on 12/8/2010

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian T. Misiura whose telephone number is (571) 272-0889. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (571) 272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Brian T Misiura/
Primary Examiner, Art Unit 2111